REMARKS

Claims 1-10 are pending in the instant application. Claims 4-6, 8 and 9 remain withdrawn. Applicant herein amends claims 1-3 and 7. (A listing of the claims is attached.)

Claims 1, 2 and 10 stand rejected under 35 U.S.C. §102 as anticipated by Hashimoto, U.S. Patent No. 6,255,842. Claims 3 and 7 stand rejected under 35 U.S.C. §103 as obvious in view of Hashimoto and Hirofumi, JP 63-082377.

Applicant respectfully traverses these rejections.

Formal Matters

The drawings are objected to. Applicant attaches corrected FIGS. 1A – 1C and 2, each now bearing a "PRIOR ART" legend and a "Replacement Sheet" mark.

Claims 3 and 7 are objected to. Claim 3 now recites, "to measure a potential difference there between." Claim 7 now recites, "the operational amplifier has ... a non-inverted input terminal that is connected to ground."

Applicant thanks the Examiner for his suggestions for corrections.

Hashimoto, U.S. Patent No. 6,255,842 ("Hashimoto")

Hashimoto's FIG. 1 is an applied-voltage-based current-measuring apparatus. The apparatus includes current measuring resistors R1, R2 and R3, all connected in series between the output terminal of the operational amplifier 12 operating as the voltage source 12 and the voltage sensing point SEN. The voltage source 12 includes an operational amplifier 12A and a D/A converter 12B. Change-over switches S4, S5, S6 and S7 are connected at one end to the ends a, b, c and d of the current measuring resistors R1, R2 and R3, respectively, and are connected together at the other end. FIG. 1 also includes an IC under Test 11. col. 1, lines 38-40; col. 5, lines 16-63; FIG. 1.

Hashimoto applies the output voltage of an operational amplifier to a voltage sensing point via a current detecting resistor, supplies a load with the voltage applied to the voltage sensing point, feeds back the voltage at the voltage sensing point to an inverting input terminal of the operational amplifier, supplies the load with a voltage identical with that fed to an non-inverting input terminal of the operational amplifier and measures current flowing to the load by a voltage which is developed across the current measuring resistor. A plurality of current detecting resistors are

prepared in correspondence to current measuring ranges. The plurality of current measuring resistors are connected in series between an output terminal of the operational amplifier and the voltage sensing point. Voltages developed at respective ends of the plurality of current detecting resistors are measured. The measured voltages are subjected to arithmetic processing to compute voltages which are created across the respective current detecting resistors, and the thus computed voltages are used to calculate the value of current flowing to the load. col. 3, lines 43-64.

Hashimoto teaches an arithmetic processing control unit 14 with a microcomputer and subtracting means for detecting potential differences V1, V2 and V3 between adjacent ends of the current measuring resistors R1, R2 and R3. col. 6, lines 7-9.

Hirofumi, JP 63-082377 ("Hirofumi")

Hirofumi is an apparatus for achieving a load-current measurement in a short time, by arranging a current-measuring circuit in a fixed voltage loop circuit provided to apply a fixed voltage to a load in parallel therewith, respective shut-off switches in parallel composing the circuit and a short-circuit switch for all thereof. Abstract.

FIG. 1 illustrates a D/A converter 16 and switches RYn connecting to the output of the op amp 14 through an element 26.

The Claimed Invention Distinguished from the Cited Art

Claim 1

As cited in the Office Action, Hashimoto does not teach or suggest "***series connections ... connected in parallel to each other***." The Office Action proposed circuits SC1-SC3 as the recited series connections. However, the one op amp 12A and the one resistor R3 are integral parts of all of the circuits SC1-SC3. But the op amp 12A and resistor R3 cannot be in parallel with themselves. Therefore, the circuits SC1-SC3 of the Office Action cannot be in parallel. Hashimoto does not teach or suggest the recited limitation of claim 1.

As cited, Hashimoto does not teach or suggest a "***current buffer with a switch***." The op amp 12A and the switches S5-S7 are all distinct components, none a part of any other. It is not immediately apparent how integrating a switch into the op amp 12A wouldn't break the Hashimoto apparatus. Hashimoto does not teach or suggest the recited limitation of claim 1.

As cited, Hashimoto does not teach or suggest a "***current buffer[which] has ... a pre-stage portion***." The Office Action proposes the op amp 12A and the D/A converter 12B as the recited

pre-stage portion. But this is incorrect. The op amp 12A and the D/A converter 12B compose the voltage source 12. Were the op amp 12A and the D/A converter 12B to compose the recited current buffer, then the Hashimoto apparatus would have no voltage source. Hashimoto does not teach or suggest the recited limitation of claim 1.

As cited, Hashimoto does not teach or suggest a "***potential difference measuring means, measuring ... a potential difference between the input side and the output side of the selected series connection***." Hashimoto merely measures potential difference between voltages such as $V3=V_a - V_b$ at input (a) and output (b) of the resistor R3. Hashimoto does not teach or suggest the recited limitation of claim 1.

Claim 3

As cited in the Office Action, neither Hashimoto nor Hirofumi nor the combination teaches or suggests a "***voltage-impressed current measuring apparatus ... wherein the input sides of the plurality of current buffers with switches of the current-range switching portion are connected to the output side of the operational amplifier***." The Office Action proposes that the limitation reads on the current measuring circuit of Hirofumi FIG. 1 and in particular the D/A converter 16 and switches RYn connecting to the output side of op amp 14 through element 26. But this is incorrect. It is impossible to introduce a current-measuring circuit of Hirofumi into Hashimoto since Hashimoto requires a arithmetic processing control unit for computing $V_a - V_b$, $V_b - V_c$ and $V_c - V_d$. Neither Hashimoto nor Hirofumi nor the combination teaches or suggests the recited limitation of claim 1.

CONCLUSION

Applicant amends the application and requests reconsideration and allowance in view of the discussion set forth above.

Respectfully submitted,

Larry Mendenhall
Reg. No. 38,555
601 California St., Suite 1111
San Francisco, CA 94108-2805
Telephone: (415) 989-8080
Facsimile: (415) 989-0910

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I certify that this Response to Office Action and all enclosed materials are being deposited with the United States Postal Service on July 20, 2007 as "Express Mail," mailing label EV 800 651 079 US, in an envelope addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Larry Mendenhall

Encl.: Listing of Claims
Replacement FIGS. 1A - 1C and 2